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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/665,171	09/19/2003	Rodney E. Hooker	CNTR.2213	6328

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EXAMINER	
PATEL, HETUL B	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 02/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/665,171	HOOKER, RODNEY E.	
	Examiner	Art Unit	
	Hetul Patel	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-46* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-46* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *09/19/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-46 are presented for examination.

2. The IDS filed on 09/19/2003 has been received and carefully considered.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 17 and 32 are rejected under 35 U.S.C. 102(e) as being anticipated by Mahalingaiah et al. (USPN: 6,389,512) hereinafter, Mahalingaiah.

As per claim 1, Mahalingaiah teaches an apparatus in a pipeline microprocessor (i.e. 12 in Fig. 1), for ensuring coherency of instructions within stages of the pipeline microprocessor, the apparatus comprising: instruction cache management logic (i.e. combination of 40, 42, 44, 46, 48, 50 in Fig. 2), configured to receive an address corresponding to a next instruction (i.e. the address corresponding to the instruction that has been fetched but not yet retired), and configured to detect that a part of a memory page corresponding to said next instruction cannot be freely accessed without checking for coherency of the instructions within said part of said memory page (i.e. addresses

corresponding to memory locations being modified are compared to the addresses stored in the core snoop buffer on a page basis) and, upon detection, configured to provide said address; and synchronization logic (i.e. combination of 40, 42, 44, 46, 48, 50 in Fig. 2), configured to receive said address from said instruction cache management logic, and configured to direct data cache management logic to check for coherency of the instructions within said part of said memory page, and, if the instructions are not coherent within said part of said memory page, said synchronization logic is configured to direct the pipeline microprocessor to stall a fetch of said next instruction until the stages of the pipeline microprocessor have executed all preceding instructions (i.e. If a match is detected, then instructions are flushed from the instruction processing pipeline and prefetched) (e.g. see the abstract and Figs. 1 and 2).

As per claims 17 and 32, Mahalingaiah teaches a method and an apparatus in a pipeline microprocessor (i.e. 12 in Fig. 1), for ensuring coherency of instructions within stages of the pipeline microprocessor, the apparatus comprising: data cache management logic (i.e. combination of 40, 42, 44, 46, 48, 50 in Fig. 2), configured to receive an address corresponding to a store instruction (i.e. the next instruction, the address corresponding to the instruction that has been fetched but not yet retired) that is pending, and configured to detect that a part of a memory page corresponding to said store instruction cannot be freely accessed without checking for coherency of the instructions within said part of said memory page (i.e. addresses corresponding to memory locations being modified are compared to the addresses stored in the core snoop buffer on a page basis) and, upon detection, configured to provide said address;

and synchronization logic (i.e. combination of 40, 42, 44, 46, 48, 50 in Fig. 2), configured to receive said address from said data cache management logic, and configured to direct instruction cache management logic to check for coherency of the instructions within said part of said memory page, and, if the instructions are not coherent within said part of said memory page, said synchronization logic is configured to direct the pipeline microprocessor to stall a fetch of said store instruction until the stages of the pipeline microprocessor have executed all preceding instructions (i.e. If a match is detected, then instructions are flushed from the instruction processing pipeline and prefetched) (e.g. see the abstract and Figs. 1 and 2).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2-16, 18-31 and 33-46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mahalingaiah in view of Kyker et al. (USPN: 2004/0015675) hereinafter, Kyker.

As per claim 2, Mahalingaiah teaches the claimed invention as described above. However, Mahalingaiah does not teach that the instruction cache management logic evaluates an instruction translation lookaside buffer (ITLB) entry corresponding to said address to detect that said part cannot be freely accessed. Kyker, on the other hand,

teaches that

"[I]n performing snoops with the ITLB 412 (referred to as "snooping"), the content addressable memory performs comparisons using the physical address of a store into the memory 104' to determine if it is associated with instructions stored within an instruction cache. If a match is found, a store occurred into memory 104' within a page of instructions that may be stored within an instruction cache. In this case, the instruction cache and the instruction pipeline may be incoherent with memory" (e.g. see paragraphs [0051]-[0052]). Accordingly, it would have been obvious to one of ordinary skilled in the art at the time of the current invention was made to modify the apparatus taught by Mahalingaiah so, the instruction cache management logic evaluate the ITLB to make sure that the part of a memory page (i.e. the smaller block of memory within a memory page) can or cannot be freely accessed because of incoherency of the instruction pipeline with memory, as taught by Kyker.

As per claim 3, the combination of Mahalingaiah and Kyker teaches the claimed invention as described above and furthermore, Kyker teaches that the ITLB entry corresponds to the memory page (e.g. see paragraph [0052]).

As per claim 4, the combination of Mahalingaiah and Kyker teaches the claimed invention as described above and furthermore, Kyker teaches that the ITLB entry comprises a plurality of part-page ownership bits (i.e. FINE HITS bits) (e.g. see paragraph [0052]).

As per claims 5 and 6, the combination of Mahalingaiah and Kyker teaches the claimed invention as described above and furthermore, Kyker teaches that one of said

plurality of part-page ownership bits (i.e. one of the FINE HITS bits) corresponds to the part of said memory page (i.e. the smaller block of memory within a memory page) and remaining ones of said plurality of part-page ownership bits correspond to remaining parts of said memory page (e.g. see paragraph [0052]).

As per claims 7 and 8, the combination of Mahalingaiah and Kyker teaches the claimed invention as described above and furthermore, Kyker teaches that the part can be freely accessed if said one of said plurality of part-page ownership bits is set; and the part cannot be freely accessed if said one of said plurality of part-page ownership bits is not set (i.e. "[T]he ITLB 412 and associated snoop logic illustrated in FIG. 6 only indicate an SMC hit if a physical match has occurred") (e.g. see paragraph [0052]).

As per claim 9, the combination of Mahalingaiah and Kyker teaches the claimed invention as described above and furthermore, Kyker teaches that the plurality of part-page ownership bits comprise four part-page ownership bits, and wherein said part comprises one-quarter of said memory page (i.e. "[T]he FINE HIT bits for simplicity are selected in the preferred embodiment to provide a granularity of 1K or 1024 addresses within a 4K page of memory. While this is the size utilized in the preferred embodiment, other granularities may be utilized. In the preferred embodiment, the ITLB 412 includes four FINE HIT bits with each line of translation contained therein, each being associated with a 1K block of addresses within a 4K page. ") (e.g. see paragraph [0052]).

As per claims 10-16, the combination of Mahalingaiah and Kyker teaches the claimed invention as described above. Kyker teaches about evaluating ITLB entry corresponding to the address to detect that the instruction is not coherent within the part

of the memory page; the ITLB entry comprises a plurality for part-page ownership bits, each corresponds to the part of the memory page; if one of said plurality for part-page ownership bits is set, the corresponding part cannot be freely accessed, as recited in rejection of claims 2-9 above. Claims 10-16 are claiming similar limitations as claims 2-9 except DTLB instead of ITLB. Since Kyker discloses that "[T]he present invention has been described herein with reference to instructions in an instruction translation lookaside buffer (ITLB) and an instruction cache, but it is equally applicable for cache coherency between memory and a cache storing data where a translation lookaside buffer is used" (e.g. see paragraph [0056]), the combination of Mahalingaiah and Kyker also teaches the limitations of claims 10-16. Based on this rationale, claims 10-16 are rejected.

As per claims 18-25, see arguments with respect to the rejection of claims 2-9, respectively. Claims 18-25 are also rejected based on the same rationale as the rejection of claims 2-9, respectively.

As per claims 26-30, see arguments with respect to the rejection of claims 2-6, respectively. Claims 26-30 are also rejected based on the same rationale as the rejection of claims 2-6, respectively.

As per claims 41-46, 40 and 33-39, see arguments with respect to the rejection of claims 2-16, respectively. Claims 41-46, 40 and 33-39 are also rejected based on the same rationale as the rejection of claims 2-16, respectively.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hetul Patel whose telephone number is 571-272-4184. The examiner can normally be reached on M-F 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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MATTHEW D. ANDERSON
PRIMARY EXAMINER